WHAT IS CLAIMED IS:

1. A Static Random Access Memory (SRAM) cell, comprising:

a pair of cross-coupled inverters forming a pair of data nodes, each cross-coupled inverter having a pull-up device and a pull-down device, said pull-down device's source terminal being biased by a select bias potential applied to a row of SRAM cells in which said SRAM cell is disposed; and

a pair of access devices, each being disposed between a respective data node and associated bitline, wherein gates of said access devices are operable to be driven by a wordline.

2. The SRAM cell as set forth in claim 1, wherein said pull-up device comprises a P-channel field-effect transistor (P-FET).

3. The SRAM cell as set forth in claim 1, wherein said pull-down device comprises an N-channel field-effect transistor (N-FET).

4. The SRAM cell as set forth in claim 1, wherein said select bias potential is operable to preserve stability of logic levels stored at said data nodes.

5. The SRAM cell as set forth in claim 1, wherein said select bias potential is operable to be decoupled from said pull-down device in a read operation.

6. The SRAM cell as set forth in claim 1, wherein biasing of said pull-down device is controlled by a logic level associated with said wordline.

7. The SRAM cell as set forth in claim 1, wherein said select bias potential is applied by biasing a body well potential of said pull-down device.

8. The SRAM cell as set forth in claim 1, wherein said select bias potential is selected to preserve stability of said SRAM cell.

9. A Static Random Access Memory (SRAM) instance, comprising:

a plurality of SRAM cells organized in an array having rows and columns, each SRAM cell including a pair of cross-coupled inverters that are coupled to form a pair of data nodes, wherein pull-down devices of said SRAM cells forming a row are coupled together to be biased by a bias potential in standby mode;

a row decoder for selectively activating wordlines based on a decoded address, wherein each wordline is operable to drive a corresponding row of said array; and

a multiplexer disposed between said row decoder and said array for deactivating said bias potential provided to said SRAM cells of a particular row when said particular row is driven by a wordline associated therewith.

10. The SRAM instance as set forth in claim 9, wherein said decoded address comprises a row address.

11. The SRAM instance as set forth in claim 9, wherein said pull-down devices of said SRAM cells comprise N-channel field-effect transistor (N-FET) devices.

12. The SRAM instance as set forth in claim 9, wherein said bias potential is approximately in a range of from about 100 millivolts to about 300 millivolts.

13. The SRAM instance as set forth in claim 9, wherein said bias potential is operable to preserve stability of logic levels stored at said data nodes of an SRAM cell.

14. The SRAM instance as set forth in claim 9, wherein said multiplexer comprises a plurality of bias switch elements, each corresponding to a wordline.

15. The SRAM instance as set forth in claim 14, wherein each bias switch element comprises logic circuitry driven by a corresponding wordline to deactivate said bias potential when said corresponding wordline is driven high.

16. The SRAM instance as set forth in claim 9, wherein said bias potential is applied by biasing a body well potential of said pull-down device.

17. The SRAM instance as set forth in claim 9, wherein said bias potential is selected to preserve stability of said SRAM cells.

18. The SRAM instance as set forth in claim 9, wherein said bias potential is applied by biasing said pull-down devices' respective source terminals.

19. A memory compiler for compiling at least one Static Random Access Memory (SRAM) memory instance, comprising:

a code portion for generating a plurality of SRAM memory cells organized in an array having rows and columns, each SRAM cell including a pair of cross-coupled inverters that are coupled to form a pair of data nodes, wherein pull-down devices of said SRAM cells forming a row are coupled together to be biased by a bias potential in standby mode;

a code portion for generating a row decoder that selectively activates wordlines based on a decoded address, wherein each wordline is operable to drive a corresponding row of said array; and

a code portion for generating a multiplexer disposed between said row decoder and said array, said multiplexer for deactivating said bias potential provided to said SRAM cells of a particular row when said particular row is driven by a wordline associated therewith.

20. The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said decoded address comprises a row address.

21. The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said pull-down devices of said SRAM cells comprise N-channel field-effect transistor (N-FET) devices.

22. The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said bias potential is approximately in a range of from about 100 millivolts to about 300 millivolts.

23. The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said bias potential is operable to preserve stability of logic levels stored at said data nodes of an SRAM cell.

24. The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said multiplexer comprises a plurality of bias switch elements, each corresponding to a wordline.

25. The memory compiler for compiling at least one SRAM memory instance as set forth in claim 24, wherein each bias switch element comprises logic circuitry driven by a corresponding wordline to deactivate said bias potential when said corresponding wordline is driven high.

26. The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said bias potential is applied by biasing a body well potential of said pull-down device.

27. The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said bias potential is selected to preserve stability of said SRAM cells.

28. The memory compiler for compiling at least one SRAM memory instance as set forth in claim 19, wherein said bias potential is applied by biasing said pull-down devices' respective source terminals.

29. A memory operation method associated with a Static Random Access Memory (SRAM) instance, said SRAM instance having a plurality of SRAM memory cells organized in an array having rows and columns, each SRAM cell including a pair of cross-coupled inverters that are coupled to form a pair of data nodes, comprising:

in standby mode, providing a bias potential to pull-down devices of said SRAM cells that form a row of said array;

selectively activating a wordline based on a decoded address for a memory read operation, said wordline for accessing a bitcell on a row of SRAM cells; and

responsive to activating said wordline, deactivating said bias potential from said pull-down devices of said row of SRAM cells.

30. The memory operation method associated with an SRAM instance as set forth in claim 29, wherein said decoded address comprises a row address.

31. The memory operation method associated with an SRAM instance as set forth in claim 30, further comprising:

selecting a particular bitline column based on a column address; and

reading a data value stored at a select bitcell selected by said row address and said column address while continuing to activate said bias potential of remaining bitcells of said particular bitline column.

32. The memory operation method associated with an SRAM instance as set forth in claim 31, wherein said bias potential is approximately in a range of from about 100 millivolts to about 300 millivolts.

33. The memory operation method associated with an SRAM instance as set forth in claim 31, further comprising, upon completion of said reading, re-activating said bias potential to said row of SRAM cells associated with said row address.

34. The memory operation method associated with an SRAM instance as set forth in claim 29, wherein said bias potential is applied by biasing a body well potential of said pull-down device.

35. The memory operation method associated with an SRAM instance as set forth in claim 29, wherein said bias potential is selected to preserve stability of said SRAM cells.

36. The memory operation method associated with an SRAM instance as set forth in claim 29, wherein said bias potential is applied by biasing said pull-down devices' respective source terminals.